In the Claims

The following Listing of Claims replaces all prior versions in the application:

LISTING OF CLAIMS

1. (Currently Amended) A pipelined averaging filter comprising:

at least one subtractor section having a plurality of adder logic units; and

at least one adder section having a plurality of adder logic units, each adder logic unit of the at least one adder section being associated with a corresponding adder logic unit of the at least one subtractor section,

wherein the at least one subtractor section and the at least one adder section are interleaved with one another such that each adder logic unit of the at least one adder section is coupled to the corresponding adder logic unit of the at least one subtractor section to thereby receive therefrom as a direct input the output of said corresponding adder logic unit of the at least one subtractor section.

2. (Original) The pipelined averaging filter as defined in claim 1, wherein the at least one adder section includes a one delay feedback for each of the plurality of adder logic units.

3. (Original) The pipelined averaging filter as defined in claim 2, wherein the averaging filter includes a delay enable signal output for each of the plurality of adder logic units of the at least one adder section.

4. (Original) The pipelined averaging filter as defined in claim 3, further comprising a delay enable signal for each delay enable signal output.

5. (Original) The pipelined averaging filter as defined in claim 1, wherein the averaging filter includes a delay enable signal output for each of the plurality of adder logic units of the at least one adder section.

6. (Original) The pipelined averaging filter as defined in claim 5, further comprising a delay enable signal for each delay enable signal output.

7. (Currently Amended) A pipelined averaging filter comprising:

at least one subtractor section having a plurality of adder logic units; and

at least one adder section having a plurality of adder logic units,

wherein the at least one adder section includes a one delay feedback for each of the plurality of adder logic units and comprises a plurality of bit segments that are different from one another.

8. (Original) The pipelined averaging filter as defined in claim 7, wherein the averaging filter includes a delay enable signal output for each of the plurality of adder logic units of the at least one adder section.

9. (Original) The pipelined averaging filter as defined in claim 8, further comprising a delay enable signal for each delay enable signal output.

10. (Original) A pipelined averaging filter comprising:

at least one subtractor section having a plurality of adder logic units; and

at least one adder section having a plurality of adder logic units,

wherein the averaging filter includes a delay enable signal output for each of the plurality of adder logic units of the at least one adder section.

11. (Original) The pipelined averaging filter as defined in claim 10, further comprising a delay enable signal for each delay enable signal output.

12. (Currently Amended) A pipelined processor comprising:

a plurality of adder logic units grouped into bit segments that are different from one another; and

a one delay feedback for each of the plurality of adder logic units.

13. (Currently Amended) A pipelined processor comprising:

a plurality of adder logic units grouped into bit segments that are different from one another; and

a delay enable signal output for each of the plurality of adder logic units.

14. (Original) The pipelined processor as defined in claim 13, further comprising a delay enable signal for each delay enable signal output.

15. (Original) The pipelined processor as defined in claim 13, further comprising a one delay feedback for each of the plurality of adder logic units.

16. (Original) The pipelined processor as defined in claim 15, further comprising a delay enable signal for each delay enable signal output.

17. (Currently Amended) A pipelined processor comprising:

at least a first processor section having a plurality of adder logic units; and

at least a second processor section having a plurality of adder logic units, each adder logic unit of the at least first processor section being associated with a corresponding adder logic unit of the at least second processor section,

wherein the at least ~~a~~ first processor section and the at least ~~a~~ second processor section are interleaved with one another such that each adder logic unit of the at least first processor section is coupled to the corresponding adder logic unit of the at least second processor section to thereby receive therefrom as a direct input the output of said corresponding adder logic unit of the at least second processor section.

18. (Original) The pipelined processor as defined in claim 17, wherein the at least a second processor section includes a one delay feedback for each of the plurality of adder logic units.

19. (Original) The pipelined processor as defined in claim 18, wherein the processor includes a delay enable signal output for each of the plurality of adder logic units of the at least a second processor section.

20. (Original) The pipelined processor as defined in claim 19, further comprising a delay enable signal for each delay enable signal output.

21. (Original) The pipelined processor as defined in claim 17, wherein the processor includes a delay enable signal output for each of the plurality of adder logic units of the at least a second processor section.

22. (Original) The pipelined processor as defined in claim 21, further comprising a delay enable signal for each delay enable signal output.

23. (Original) A method of pipelined processing an n-bit word, the method comprising:

dividing the n-bit word into a plurality of bit segments;

generating a delay enable signal for each of the plurality of bit segments;

processing the plurality of bit segments; and

applying the delay enable signal to each of the processed plurality of bit segments to assemble the output of the pipelined processing.

24. (Original) The method as defined in claim 23, wherein the plurality of bit segments are of equal length.

25. (Original) The method as defined in claim 23, wherein processing comprises applying a one delay feedback to each of the plurality of bit segments.

26. (Original) The method as defined in claim 25, wherein processing comprises a first processor section and a second processor section, wherein the first processor section and the second processor section are interleaved with one another.

27. (Original) The method as defined in claim 23, wherein processing comprises a first processor section and a second processor section, wherein the first processor section and the second processor section are interleaved with one another.

28. (Original) A pipelined processor for an n-bit word, the processor comprising:

means for dividing the n-bit word into a plurality of bit segments;

means for generating a delay enable signal for each of the plurality of bit segments;

means for processing the plurality of bit segments; and

means for applying the delay enable signal to each of the processed plurality of bit segments to assemble the output of the pipelined processor.

29. (Original) The pipelined processor as defined in claim 28, wherein the plurality of bit segments are of equal length.

30. (Original) The pipelined processor as defined in claim 28, wherein means for processing comprises means for applying a one delay feedback to each of the plurality of bit segments.

31. (Original) The pipelined processor as defined in claim 30, wherein means for processing comprises a first processor section and a second processor section, wherein the first processor section and the second processor section are interleaved with one another.

32. (Original) The pipelined processor as defined in claim 28, wherein means for processing comprises a first processor section and a second processor section, wherein the first processor section and the second processor section are interleaved with one another.